AF RJ

DOCKET NO. 98-MET-069C1 (STMI01-01012) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	David L. Isaman
U.S. Serial No.	:	09/443,160
Filed	:	November 19, 1999
For	:	SYMBOLIC STORE-LOAD BYPASS
Group No.	:	2183
Examiner	:	Daniel H. Pan

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Sir:

The undersigned hereby certifies that the following documents:

1. Response to Notice of Non-Compliant Appeal Brief; and
2. Postcard receipt

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to MAIL STOP APPEAL BRIEF - PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 16, 2007.

Date: November 16, 2007 Rita Kaur
Mailer

Date: 16 Nov. 2007 John T. Mockler
John T. Mockler
Reg. No. 39,775

P.O. Box 802432
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *jmockler@munckbutrus.com*

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RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF

In response to the Notice of Non-Compliant Appeal Brief dated October 16, 2007, the Applicant is submitting this Response in accordance with the guidelines in M.P.E.P. §1205.03(B).

In the October 16, 2007 Notice of Non-Compliant Appeal Brief, the Examiner asserted that the Substitute Appeal Brief filed on June 20, 2007 failed to comply with 37 C.F.R. §41.37(c)(1)(v) in that the Appeal Brief did not contain a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number and to the drawings by reference characters.

The Appellant respectfully disagrees with the Examiner's assertions regarding the alleged

shortcomings of the June 20, 2007 Substitute Appeal Brief.

The Appellant notes that independent Claim 2 was concisely explained from the bottom of page 7 through page 8. The Claim 2 explanation is only a page and a quarter long, including the insertions of the required references to the specification (page and line numbers) and drawings (reference numbers). During a teleconference with the Examiner, when the undersigned asked for an explanation for the alleged lack of concision, the Examiner explained unhelpfully that "we don't feel this is concise", without further elaboration. The Examiner gave similar unhelpful explanations regarding the alleged lack of concision of independent Claims 12 and 20.

Nonetheless, in order to move the prosecution of the present application along, the Appellant will attempt again to provide the required summary of the claimed subject matter in compliance with 37 §CFR 41.37(c)(1)(v). The Appellant notes that another substitute Appeal Brief is not required. In M.P.E.P. §1205.03(B), it states that "When the Office holds the brief to be defective solely due to appellant's failure to provide a summary of the claimed subject matter as required by 37 CFR 41.37(c)(1)(v), an entire new brief need not, and should not, be filed. Rather, a paper providing a summary of the claimed subject matter as required by 37 CFR 41.37(c)(1)(v) will suffice." Accordingly, the Appellant is submitting this Response in order to provide the required summary of the claimed subject matter

SUMMARY OF CLAIMED SUBJECT MATTER

CLAIM 2

Claim 2 states in its entirety:

> 2. A pipelined microprocessor capable of detecting an instruction that loads data from a first memory location that was previously stored to, wherein the instruction is detected without requiring computation of an external memory address of said first memory location for the instruction.

The Appellant respectfully asserts that the following is a concise explanation of the subject matter defined in independent Claim 2. Claim 2 is directed to a pipelined microprocessor 100 that detects an instruction 151 that loads data from a first memory location to which data was previously stored. The instruction 151 is detected without requiring computation of an external memory address of the first memory location for the instruction 151. The microprocessor 100 is shown in Figure 1 and is described throughout the specification. However, the text of the specification from page 8, line 20, to page 9, line 22, gives a detailed explanation regarding the microprocessor 100 and the operation by which the microprocessor 100 determines that a load instruction 151 will read data from the same memory location to which a store instruction 151 had written the data. See Specification, page 9, lines 13-22. The microprocessor 100 instead uses the data from an internal register, rather than waiting for an external memory to complete the store and load operations, thereby increasing the speed of the microprocessor 100. See Specification, page 9, lines 13-22.

CLAIM 12

Claim 12 states in its entirety:

> 12. A method for operating a pipelined microprocessor, said method comprising:
>
> detecting in said pipelined microprocessor an instruction that loads data from a first memory location that was previously stored to, wherein the instruction is detected without requiring computation of an external memory address of said first memory location for the instruction.

The Appellant respectfully asserts that the following is a concise explanation of the subject matter defined in independent Claim 12. Claim 12 is directed to a method for operating a pipelined microprocessor 100. The method comprises the step of detecting in the pipelined microprocessor 100 an instruction 151 that loads data from a first memory location to which the data was previously stored. The step of detecting the instruction 151 is performed without requiring computation of an external memory address of the first memory location for the instruction 151. The microprocessor 100 is shown in Figure 1 and is described throughout the specification. However, the text of the specification from page 8, line 20, to page 9, line 22, gives a detailed explanation regarding the microprocessor 100 and the operation by which the microprocessor 100 determines that a load instruction 151 will read data from the same memory location to which a store instruction 151 had written the data. See Specification, page 9, lines 13-22. The microprocessor 100 instead uses the data from an internal register, rather than waiting for an external memory to complete the store and load operations, thereby increasing the speed of the microprocessor 100. See Specification, page 9, lines 13-22.

Additionally, the method of Claim 12 is described with respect to the flow diagram in

Figures 2A and 2B, and in particular with respect to steps 217 through steps 226 described from line 8, page12, through line 8, page 14, of the Specification.

CLAIM 20

Claim 20 states in its entirety:

> 20. A method for operating a pipelined microprocessor, said method comprising:
>
> detecting a first instruction that stores data to a first memory location, said first instruction comprising syntax for computing an effective address for said first memory location;
>
> detecting a second instruction that loads data from a second memory location, said second instruction comprising syntax for computing an effective address for said second memory location;
>
> determining said syntax for said first instruction and said syntax for said second instruction;
>
> using said syntax for said first instruction and said syntax for said second instruction to determine a relationship between said first memory location and said second memory location, without requiring computation of said effective address for said first memory location and without requiring computation of said effective address for said second memory location; and
>
> using said relationship to determine whether to perform one of said first instruction and said second instruction.

The Appellant respectfully asserts that the following is a concise explanation of the subject matter defined in independent Claim 20. Claim 20 is directed to a method for operating a pipelined microprocessor 100. The method comprises the steps of detecting a first instruction 151 that stores data to a first memory location, where the first instruction 151 comprises syntax for computing an effective address for the first memory location. This step is shown in steps 213-216 of Figure 2A and explained in the Specification from line 8, page 11 through line 6, page 12. The step of "detecting a second instruction 151 that loads data from a second memory

location, [the] second instruction 151 comprising syntax for computing an effective address for [the] second memory location" is also shown and explained in steps 213-216 of Figure 2A.

The Claim 20 step of "determining [the] syntax for [the] first instruction 151 and [the] syntax for [the] second instruction 151" is shown in step 213 of Figure 2A and explained at lines 8-13 of page 11 of the Specification. The Claim 20 method uses the syntax for the first and second instructions 151 to determine if the first and second memory locations are the same, without requiring computation of the effective addresses for the first and second memory locations. See Figure 2, steps 217, 220, 226 and Specification, page 12, line 8, to page 13, line 2, and page 14, lines 1-8. If the first and second memory locations are the same, the Claim 12 method determines whether to perform one of the first and second instructions. See Figure 2, steps 217, 220, 226 and Specification, page 12, line 8, to page 13, line 2, and page 14, lines 1-8.

REMARKS

The Appellant respectfully submits that the concise explanations provided above for Claims 2, 12 and 20 are more than adequate to meet the requirements of 37 CFR 41.37(c)(1)(v). Accordingly, the Appellant respectfully requests issuance of an Examiner's Answer responding to the merits of the Appellant's Substitute Appeal Brief so that this application can proceed towards a final decision on appeal.

If any outstanding issues remain or if the Examiner has any suggestions for expediting allowance of this application, the Appellant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@munckbutrus.com*.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS CARTER, P.C.

Date: 16 Nov. 2007

John T. Mockler
Registration No. 39,775

Docket Clerk
P.O. Box 802432
Dallas, Texas 75380
Tel: (972) 628-3600
Fax: (972) 628-3616
Email: *jmockler@munckbutrus.com*